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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/849,958	TAKAHASHI, HITOSHI	
	Examiner	Art Unit	
	Hyun Nam	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 5 and 10 are rejected under 35 U.S.C. 101 because the scope of the claim encompasses inventions that lack patentable utility.

In claim 5, the limitation 'a flip-flop' includes D flip-flop, one of commonly known flip-flops in the art. An embodiment of the invention with D flip-flop will produce a Q output state of logic one when the pulse signal is received at the latched terminal as claimed; hence, output of inverted buffer will be logic zero. This also means that the output of the AND gate mentioned in the claims will be logic zero. If the output of D flip-flop is to maintain logic one as claimed then the output of the AND gate will always be logic zero no matter what value is generated by the Control Signal Generator. Moreover, if the pulse signal at the latched terminal in D flip-flop is construed as the clock input then D input must be tied permanently to logical one. If the pulse signal at the latched terminal is construed as the D input then the clock input must never occur because it will latch in logic zero which contradicts one of the functions claimed on the invention. This is not a write protection circuit as claimed because the data it suppose to protect from the Control Signal Generator will never get latched; hence, never get protected. As claimed, the invention has no utility.

Claim 10 also uses the limitation 'a flip-flop'. Again, the embodiment of the invention with D flip-flop will not allow invention to function as claimed because D flip-flop does not have set/reset terminals. As claimed, the invention has no utility.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Use of the word 'flip-flop' in claims 5 and 10 fails to particularly point out and distinctly claim the subject matter because type of flip-flops used will determine state of the claim invention to be enabled, disabled, or indefinite. For the purpose of this examination, the limitation 'flip-flop' will be construed to mean "S/R flip-flop".

Claim 5 recites the limitation "the latch terminal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Use of the phrase 'the latch terminal' in claims 5 and 10 fails to particularly point out and distinctly claim the subject matter because the phrase does not distinguish which of the various terminals that are on flip-flops or latches (i.e., clock, input, or

output). For the purpose of this examination, the limitation 'latch terminal' will be construed to mean "a clock terminal".

Use of the phrase 'the control circuit sets' in claims 7-10 fails to particularly point out and distinctly claim the subject matter because of dual meaning and function of the word sets. For the purpose of this examination, the limitation 'the control circuit sets' will be construed to mean "the control circuit".

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-9, 11, 12, 14, 16-18, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wakasugi (U.S. Patent Number 4,228,502).

With respect to claim 1, Wakasugi teaches a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the microcomputer comprising:

an input and output circuit having a plurality of operation modes (see Figure 1);

a control signal generator (see Figure 3) for generating a write signal (see Figure 1 interface bus line 8) in an operation mode setting routine of the control program (see Figure 1 Main Memory 2);

a control circuit (see Figure 3) for setting an operation mode of the input and output circuit in response to the write signal (see Figure 1); and

a protection circuit (see Figure 3 trigger flip-flops 34, and 35) for protecting the input and output circuit from being reset in operation mode until the protection circuit is reset by the reset signal from the outside once the control circuit has set the operation mode (see Figure 3 mode switch 31),

wherein the input and output circuit receives a signal from and sends a signal to the outside in accordance with the operation mode set by the control circuit (see Figure 3 Register 39, a pointer to initial program; and Register 381 and 382, pointers to other programs).

With respect to claim 2, Wakasugi teaches an operation mode control circuit in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Figure 3);

a write protection circuit (see Figure 3) for generating a buffer signal in response to only a first output signal (see Figure 3 Register 39 output; Note, this register holds an index address of the initial program on Main Memory) the control signal generator

outputs first subsequent to the reset (see Figure 3 reset switch 32) of the microcomputer (see Figure 1); and

a control circuit (see Figure 3) for latching a second output signal (see Figure 3 Register 381 output; Note, this register holds index address of the program other then the initial program on Main Memory) from the control signal generator in response to the buffer signal from the write protection circuit,

wherein the control circuit sets an operation mode of an input and output circuit, which receives a signal from and sends a signal to the outside, in accordance with the latched second output signal (see Column 2 Line 54-61; Note, an index address from Register 381 transfers to the register 40).

With respect to claim 3, Wakasugi teaches an operation mode control circuit as claimed in claim 2, wherein the first output signal comprises a pulse signal (see Figure 3 switch 32; Note, a square pulse).

With respect to claim 4, Wakasugi teaches an operation mode control circuit as claimed in claim 2, wherein the write protection circuit comprises:

buffer units (see Figure 3 gates, flip-flops and Registers; Note, the flip-flops and Registers are made up from various combination of gates, electronic switches that performs Boolean operations, which allows signals to propagate or buffer to next device) for outputting a buffer signal that is a buffered version of the first output signal or

a fixed logical value signal in response to the first output signal output from the control signal generator; and

latch units (see Figure 3 flip-flops and Registers) for performing a latch process in response to the first output signal from the control signal generator and for outputting a status signal indicating a latch status thereof,

wherein the buffer units has an input terminal (see Figure 3 gate A30) for receiving the status signal (see Figure 3 Register 39; Note, the output line of registers in the figure represents both the status, data availability, and the content transfer, an indexed address) from the latch units, and outputs the fixed logical value signal (see Figure 3 Register 39; Note, the output line of registers indicate data availability) if the status signal indicates the latch status (see Column 2 Line 54-61), or outputs the buffer signal if the status signal does not indicate the latch status.

With respect to claim 6, Wakasugi teaches a microcomputer, comprising:

an operation mode control circuit (see Figure 1), wherein the operation mode control circuit includes a control signal generator (see Figure 3), a write protection circuit (see Figure 3) for generating a buffer signal in response to only a first output signal (see Figure 3 Register 39 output) the control signal generator outputs first subsequent to the reset (see Figure 3 reset switch 32) of the microcomputer (see Figure 1), and a control circuit (see Figure 3) for latching a second output signal (see Figure 3 Register 381 output) from the control signal generator in response to the buffer signal from the write protection circuit;

an input and output circuit for receiving a signal from and sending a signal to the outside (see Figure 1); and

a data register (see Figure 3 Register 39) for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit,

wherein the data register outputs, to the input and output circuit, a signal responsive to the data signal (see Figure 1; Note, it is inherent that Arithmetic Operation Unit handles various operation modes and controls its registers).

With respect to claim 7, Wakasugi teaches an operation mode control circuit in a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Figure 3);

a write protection circuit (see Figure 3) for generating a buffer signal that is a buffered version of a first output signal (see Figure 3 gate A30; Note, a signal from AND gate output) from the control signal generator only if a first decode signal (see Figure 3 Register 39; Note, content is a decoded address or index address) and a second decode signal (see Figure 3 Register 381; Note, content is a decoded address or index address) have been successively received from the control signal generator; and

a control circuit (see Figure 3) for latching a second signal (see Figure 3 Register 381 and Register 40; Note, when index address from Register 381 moves to Register

40) from the control signal generator in response to the buffer signal from the write protection circuit,

wherein the control circuit sets, in response to the second output signal latched, the operation mode of an input and output control circuit that receives a signal from and sends a signal to the outside (see Figure 3).

With respect to claim 8, Wakasugi teaches an operation mode control circuit as claimed in claim 7, wherein the first output signal comprises a pulse signal (see Figure 3 switch 32; Note, a square pulse).

With respect to claim 9, Wakasugi teaches an operation mode control circuit in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Figure 3);

a write protection circuit (see Figure 3) for generating a buffer signal that is a buffered version of a first output signal (see Figure 3 gate A30; Note, a signal from AND gate output) from the control signal generator only if a plurality of decode signals (see Figure 3 Register 39 and 381; Note, contents are decoded addresses or index addresses) have been successively received from the control signal generator; and

a control circuit (see Figure 3) for latching a second signal (see Figure 3 Register 381 and Register 40; Note, when index address from Register 381 moves to Register

40) from the control signal generator in response to the buffer signal from the write protection circuit;

wherein the control circuit sets, in response to the second output signal latched, the operation mode of an input and output control circuit that receives a signal from and sends a signal to the outside (see Figure 3).

With respect to claim 11, Wakasugi teaches a microcomputer comprising:

an operation mode control circuit (see Figure 1), wherein the operation mode control circuit includes a control signal generator (see Figure 3), a write protection circuit (see Figure 3) for generating a buffer signal that is a buffered version of a first output signal (see Figure 3 gate A30; Note, a signal from AND gate output) from the control signal generator only if a first decode signal (see Figure 3 Register 39; Note, content is a decoded address or index address) and a second decode signal (see Figure 3 Register 381; Note, content is a decoded address or index address) have been received from the control signal generator, and a control circuit (see Figure 3) for latching a second signal (see Figure 3 Register 381 and Register 40; Note, when index address from Register 381 moves to Register 40) from the control signal generator in response to the buffer signal from the write protection circuit;

an input and output control circuit (see Figure 1) for controlling signal inputting from and signal outputting to the outside; and

a data register (see Figure 3 Register 39) for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit,

wherein the data register outputs a signal responsive to the data signal to the input and output control circuit (see Figure 1; Note, it is inherent that Arithmetic Operation Unit handles various operation modes and controls its registers).

With respect to claim 12, Wakasugi teaches an operation mode control circuit in a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Figure 3);

a write protection circuit (see Figure 3) for latching a second output signal (see Figure 3 flip-flop 33 output) from the control signal generator in response to a first output signal (see Figure 3 switch 32 output) from the control signal generator, and for generating a write signal (see Figure 3 switch 31 output) responsive to the logical value of the latched second output signal (see Figure 3 flip-flop 34; Note, T input); and

a control circuit (see Figure 3) for latching a third output signal (see Figure 3 flip-flop 34 output) from the control signal generator in response to the write signal and for generating a control signal (see Figure gate A31 output) responsive to the logical value of the latched third output signal,

wherein the write signal responsive to the logical value of the second output signal from the control signal generator is a signal with the logical value fixed (see

Figure 3 switch 31) or a buffer signal that is the buffered version of the first output signal from the control signal generator, and

wherein the control signal is supplied to a selection circuit (see Figure 3 gate O30; Note, OR gate) that selects one signal generator from among a plurality of signal generators, each containing at least a data register, for sending a signal to the outside.

With respect to claim 14, Wakasugi teaches an operation mode control circuit as claimed in claim 12, wherein the write protection circuit comprises:

buffer units (see Figure 3 gates, flip-flops and Registers) for outputting one of the buffer signal resulting from the first output signal and the signal having the fixed logical value in response to the first output signal from the control signal generator, and latch units (see Figure 3 flip-flops and Registers) for latching the second output signal from the control signal generator in response to the buffer signal and outputting a logical signal responsive to the logical value of the second output signal,

wherein the buffer units receives the logical signal from the latch units (see Figure 3 gate A31 and Register 381), and outputs a signal with the logical value thereof fixed in response to one logical value of the logical signal while outputting the buffer signal in response to the other logical value of the logical signal (Note, gate A31 has multiple terminal to handle plurality of logical signals).

With respect to claim 16, Wakasugi teaches a microcomputer comprising:

an operation mode control circuit (see Figure 2), wherein the operation mode control circuit includes a control signal generator (see Figure 4), a write protection circuit (see Figure 4) for latching a second output signal (see Figure 4 flip-flop 45 output) from the control signal generator in response to a first output signal (see Figure 4 flip-flop 371 output) from the control signal generator and generating a write signal (see Figure 4 gate A30 output) responsive to the logical value of the latched second signal, a first control circuit (see Figure 4 gates A30 and O31) for latching a third output signal (see Figure 4 Register 40 input) from the control signal generator in response to the write signal and for generating a first control signal (see Figure 4 Register 39 output) responsive to the logical value of the latched third output signal, a second control circuit (see Figure 4 gates O30 and O31) for latching a fifth output signal (see Figure 4 Register 40 input) from the control signal generator in response to a fourth output signal (see Figure 4 gate O30 output) from the control signal generator, and for generating a second control signal (see Figure 4 Registers 381 or 382 output) responsive to the logical value of the latched fifth output signal, and an OR gate (see Figure 4 gate O31; Note, Figure 4 is a block diagram that simultaneously represents concepts of logic circuit and data flow) for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal (Note, Register 40 either holds index address for initial loading program or other programs);

a signal input and output control circuit (see Figure 2) for controlling of signal inputting from and signal outputting to the outside;

a data register (see Figure 3 Register 39) for latching a data signal from the operation mode control circuit in response to a data register write signal from the operation mode control circuit;

a timer for generating a clock (see Figure 4 timer 43) with at least one constant period; and

a selection circuit (see Figure 4 gate O31) for selecting one of the data register and the timer in response to the first control signal from the operation mode control circuit,

wherein the data register outputs a signal responsive to the data signal to the signal input and output control circuit (see Figure 2).

With respect to claim 17, Wakasugi teaches an operation mode control circuit of a microcomputer for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Figure 4);

a write protection circuit (see Figure 4) that outputs a buffer signal (see Figure 4 flip-flop 44 output) that is a buffered version of a first output signal (see Figure 4 Fall Detecting Circuit 44 output) from the control signal generator when a step (see Figure 4 timer 43 and Column 3 Line 18) prior to a predetermined initialization routine phase (see Column 3 Line 23) is in progress subsequent to the commencement of an initialization program (see Column 3 Line 34-37) while outputting a fixed signal (see Figure 4 Register 39 and Column 4 Line 13-15) in the rest of the time; and

a control circuit (see Figure 4) for latching a second output signal (see Figure 4 flip-flop 371 output) from the control signal generator in response to the output signal from the write protection circuit,

wherein the control circuit sets an operation mode of an input and output control circuit (see Figure 2) that controls signal inputting from and signal outputting to the outside in response to the latched second output signal.

With respect to claim 18, Wakasugi teaches an operation mode control circuit as claimed in claim 17, wherein the first output signal from the control signal generator comprises a pulse signal (see Figure 4 switch 32 output).

With respect to claim 20, Wakasugi teaches a microcomputer comprising:

an operation mode control circuit (see Figure 2), wherein the operation mode control circuit includes a control signal generator (see Figure 4), a write protection circuit (see Figure 4) that outputs a buffer signal (see Figure 4 flip-flop 45 output) that is a buffered version of a first output signal (see Figure 4 Fall Detecting Circuit 44 output) from the control signal generator when a step (see Figure 4 timer 43 and Column 3 Line 18) prior to a predetermined initialization routine phase (see Column 3 Line 23) is in progress subsequent to the commencement of an initialization program (see Column 3 Line 34-37) while outputting a fixed signal in the rest of the time (see Figure 4 Register 39 and Column 4 Line 13-15), and a control circuit (see Figure 4) for latching a second

output signal from the control signal generator in response to the output signal from the write protection circuit;

an input and output control circuit (see Figure 2) for controlling signal inputting from and signal outputting to the outside; and

a data register (see Figure 4 Register 39) for latching a data signal (see Column 2 Line 48-49) from the operation mode control circuit in response to a data register write signal from the operation mode control circuit (see Figure 2 Arithmetic Operation Unit 1; Note, it is inherent that the data register write signal comes from control circuit),

wherein the data register outputs a signal (see Figure 4 Register 39 output) responsive to the data signal to the input and output control circuit (see Figure 2 Keyboard 6 and Floppy Disk Unit 7).

With respect to claim 21, Wakasugi teaches a control system comprising:

a microcomputer (see Figure 2), wherein the microcomputer includes an input and output circuit (see Figure 2 Keyboard 6 and Floppy Disk Unit 7) having a plurality of operation modes,

a control signal generator (see Figure 2) for generating a write signal (see Figure 2) in an operation mode setting routine of the control program (see Column 3 Line 34-37), a control circuit (see Figure 2) for setting an operation mode of the input and output circuit in response to the write signal (see Column 4 Line 13-15), and a protection circuit for protecting the input and output circuit from being reset in operation mode until the protection circuit is reset by a reset signal from the outside once the control circuit has

set the operation mode (see Column 3 Line 17-24), a monitoring signal output port (see Figure 4 timer 43 output) for outputting a monitoring signal to the watchdog timer, a reset signal input port (see Figure 4 timer 43 input) for receiving a first reset signal (see Figure 4 timer 43 output) from the watchdog timer, and a reset circuit for generating a second reset signal (see Figure 4 Fall Detecting Circuit 44 output) to be output to a predetermined circuit (see Figure 4 flip-flop 45) of the microcomputer in response to the first reset signal; and

a watchdog timer (see Figure 4 timer 43),

wherein the output from the input and output control circuit comprises the monitoring signal supplied to the watchdog timer (see Column 3 Line 17-18), and

wherein the watchdog timer outputs the first reset signal to the microcomputer (see Column 3 Line 19).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 10, 13, 15, and 19 are rejected under 35 U.S.C. 103(a) as obvious over Wakasugi.

With respect to claim 5, Wakasugi teaches an operation mode control circuit as claimed in claim 2.

But Wakasugi does not specifically teach an operation mode control circuit as claimed in claim 2 wherein the write protection circuit comprises:

an AND gate for receiving the first output signal from the control signal generator at one of input terminals thereof;

a flip-flop, with the latch terminal thereof connected to an output terminal of the AND gate, for outputting a signal having a logical signal "1" when a pulse signal is received at the latch terminal thereof; and

a buffer for outputting a logically inverted version of a signal from the flip-flop to the other of the input terminals of the AND gate,

wherein the AND gate AND gates the first output signal from the control signal generator and the logically inverted version of the signal from the flip-flop.

However, it is commonly known in the art to utilize AND gates to sum up (using Boolean logic) plurality of signals and to apply proper signal to clock terminal of flip-flops to inhibit clearing of latched data for duration of various clock cycles. Also, it is well known in the art that logic gates such as inverters, OR gates, and AND gates (Note, a simple way to conceive that OR and AND gates are buffers is to short plurality of its input to one signal) are simultaneously used as buffers to further propagate signals to other logic devices. Once the inventor determine total logic of the device (i.e. Minterm, Maxterm, Truth Table, and Canonical Forms) various combination of gates would be a design choice.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate commonly known technique of using logic gates and flip-flops to build an operation mode control circuit taught by Wakasugi. One of ordinary skill in the art would be motivated to do because integrated circuit such as the 7400 series or 4000 series are logic building blocks that can wired together in fairly easy manner so that one can realize his/her design ideas in a shorter amount of time where high production volumes are not required.

With respect to claim 10, Wakasugi teaches an operation mode control circuit as claimed in claim 7.

But Wakasugi does not specifically teach an operation mode control circuit as claimed in claim 7, wherein the write protection circuit comprises:

a decoder for outputting a first selection status signal and a second selection status signal in response to the first decode signal and the second decode signal from the control signal generator, respectively;

a first AND gate for receiving the first selection status signal at one of input terminals thereof;

a second AND gate for receiving the second selection status signal at one of input terminals thereof;

a third AND gate;

a first flip-flop for latching an output signal from the first AND gate in response to the first output signal from the control signal generator and for outputting first data to the other of the input terminals of the second AND gate;

a second flip-flop for latching an output from the second AND gate in response to the first output signal from the control signal generator and for outputting second data to one of input terminals of the third AND gate; and

a buffer for outputting, to the other of the input terminals of the first AND gate, a third output signal that is a logically inverted version of the second data,

wherein the first AND gate AND gates the first election status signal and the third output signal,

wherein the second AND gate AND gates the second selection status signal and the first data,

wherein the third AND gate AND gates the second data and the first output signal, and

wherein the control circuit includes a third flip-flop that latches the second output signal from the control signal generator in response to an output signal from the third AND gate.

However, it is commonly known in the art to utilize Address Decoders to access memory/registers, and utilize AND gates to sum up (using Boolean logic) plurality of signals. Also, it is well known in the art that logic gates such as inverters, OR gates, and AND gates are simultaneously used as buffers to further propagate signals to other logic devices. Once the inventor determine total logic of the device (i.e. Minterm,

Maxterm, Truth Table, and Canonical Forms) various combination of gates would be a design choice.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate commonly known technique of using logic gates, flip-flops, and address decoders to build an operation mode control circuit taught by Wakasugi. One of ordinary skill in the art would be motivated to do because integrated circuit such as the 7400 series or 4000 series are logic building blocks that can wired together in fairly easy manner so that one can realize his/her design ideas in a shorter amount of time where high production volumes are not required.

With respect to claim 13, Wakasugi teaches an operation mode control circuit, in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

a control signal generator (see Figure 3);

a write protection circuit (see Figure 3) for latching a second output signal (see Figure 3 flip-flop 33 output) from the control signal generator in response to a first output signal (see Figure 3 switch 32 output) from the control signal generator and generating a write signal responsive to the logical value of the latched second signal;

a first control circuit (see Figure 3 flip-flop 34) for latching a third output signal (see Figure 3 flip-flop 34 output) from the control signal generator in response to the

write signal and for generating a first control signal responsive to the logical value of the latched third output signal; and

a second control circuit (see Figure 3 flip-flop 35) for latching a fifth output signal (see Figure 3 flip-flop 35 output) from the control signal generator in response to a fourth output signal from the control signal generator, and for generating a second control signal responsive to the logical value of the latched fifth output signal.

But Wakasugi does not specifically teach an operation mode control circuit, in a microcomputer, resettable by a reset signal from the outside, for performing processes under the control of a control program, the operation mode control circuit comprising:

an OR gate for OR gating the first control signal and the second control signal and outputting an OR gate output as an operation mode setting signal,

wherein the write signal responsive to the logical value of the second output signal from the control signal generator is a signal with the logical value thereof fixed or a buffer signal that is a buffered version of the first output signal from the control signal generator,

wherein the first control signal is supplied to a selection circuit that selects one signal generator from among a plurality of signal generators, each containing at least a data register, for sending a signal to the outside, and

wherein the operation mode setting signal is supplied to a circuit, which controls signal inputting from and signal outputting to the outside, to set the operation mode of the circuit.

However, it is commonly known in the art to utilize OR gates or MUX to select one signal (using proper Boolean logic) from plurality of signals. Also, it is well known in the art that logic gates such as inverters, OR gates, and AND gates are simultaneously used as buffers to further propagate signals to other logic devices. Once the inventor determine total logic of the device (i.e. Minterm, Maxterm, Truth Table, and Canonical Forms) various combination of gates and where the signal selection occurs within the circuits would be a design choice.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate commonly known technique of using logic gates, and flip-flops to build an operation mode control circuit taught by Wakasugi. One of ordinary skill in the art would be motivated to do because integrated circuit such as the 7400 series or 4000 series are logic building blocks that can wired together in fairly easy manner so that one can realize his/her design ideas in a shorter amount of time where high production volumes are not required.

With respect to claim 15, Wakasugi teaches an operation mode control circuit as claimed in claim 12.

But Wakasugi does not specifically teach an opration mode control circuit as claimed in claim 12, wherein the write protection circuit comprises:

an AND gate for receiving, at one of input terminals thereof, the first output signal from the control signal generator;

a buffer for outputting a buffer signal that is an logically inverted version of the second output signal from the control signal generator; and a latch for receiving the buffer signal at a data terminal thereof, for latching the buffer signal in response to an output from the AND gate, and for generating a logical signal responsive to the logical value of the buffer signal,

wherein the AND gate AND gates the logical signal and the first output signal.

However, it is commonly known in the art to utilize AND gates to sum up (using proper Boolean logic) plurality of signals. Also, it is well known in the art that logic gates such as inverters, OR gates, and AND gates are simultaneously used as buffers to further propagate signals to other logic devices. Once the inventor determine total logic of the device (i.e. Minterm, Maxterm, Truth Table, and Canonical Forms) various combination of gates would be a design choice.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate commonly known technique of using logic gates and flip-flops to build an operation mode control circuit taught by Wakasugi. One of ordinary skill in the art would be motivated to do because integrated circuit such as the 7400 series or 4000 series are logic building blocks that can wired together in fairly easy manner so that one can realize his/her design ideas in a shorter amount of time where high production volumes are not required.

With respect to claim 19, Wakasugi teaches an operation mode control circuit as claimed in claim 17, wherein the write protection circuit comprises:

a first status signal generator (see Figure 4 timer 43 output) for generating a first status signal indicating that the initialization program is in progress; and

a second status signal generator (see Figure 4 switch 32 output) for generating a second status signal indicating that the step prior to the predetermined initialization routine phase is in progress.

But Wakasugi does not specifically teach an operation mode control circuit as claimed in claim 17, wherein the write protection circuit comprises:

a first AND gate for AND gating the first status signal and the second status signal;

a set-reset flip-flop for outputting a signal having a logical value of "1" in a reset state while outputting a signal having a logical value of "0" when the output from the first AND gate is a predetermined signal; and

a second AND gate for AND gating the first output signal from the control signal generator and the output signal from the set-reset flip-flop.

However, it is commonly known in the art to utilize AND gates to sum up (using proper Boolean logic) plurality of signals and SR flip-flops to latch in state of various gate outputs. Once the inventor determine total logic of the device (i.e. Minterm, Maxterm, Truth Table, and Canonical Forms) various combination of gates and latches would be a design choice.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate commonly known technique of using logic gates and flip-flops to build an operation mode control circuit taught by Wakasugi. One

of ordinary skill in the art would be motivated to do because integrated circuit such as the 7400 series or 4000 series are logic building blocks that can wired together in fairly easy manner so that one can realize his/her design ideas in a shorter amount of time where high production volumes are not required.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hyun Nam whose telephone number is (512) 270-1725. The examiner can normally be reached on Monday through Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson, can be reached on 571-272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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